Claims:

1. (Previously Amended) In a semiconductor device having at least an insulating gate dielectric layer and a gate fabricated upon a semiconductor substrate, a buried channel implanted below the insulating gate dielectric layer, the buried channel being doped with a predetermined dopant and a peak concentration of the dopant positioned at a selected level in the substrate below the insulating gate dielectric layer to cause the substrate portions above the selected level to act as a supplemental gate dielectric layer so that when the gate is biased with respect to the substrate, the buried channel is partially depleted of charge carriers, effectively increasing the thickness of the insulating gate dielectric layer.

2. (original) The device of claim 1 wherein the substrate is a p-type substrate and the buried channel is an n-type buried channel.

3. (original) The device of claim 1 wherein the substrate is an n-type substrate and the buried channel is a p-type channel.

4. (original) The device of claim 2 wherein the bias from the gate to the substrate is an inversion bias.

5. (original) The device of claim 3 wherein the bias from the gate to the substrate is an inversion bias.

6. (original) The device of claim 1 wherein the device is an NMOS transistor.

7. (original) The device of claim 1 wherein the device is a PMOS transistor.

8. (original) The device of claim 1 wherein the device is a MOS capacitor.

9. (original) The device of claim 8 wherein the MOS capacitors comprise part of a one transistor random access memory.

10-21. (cancelled)

22. (previously added) The semiconductor device of claim 1, wherein the insulating gate dielectric layer and the substrate forms an interface and the peak concentration of implanted dopants in the buried channel is located between 400 and 1000 Angstroms below the interface.

23. (previously added) An integrated circuit fabricated on a semiconductor substrate and having at least two devices, each of the devices having a different effective gate oxide thickness, the circuit comprising:

a first device having a gate disposed on a gate dielectric layer, the gate dielectric layer having a first thickness and a first effective gate dielectric value and disposed on the semiconductor substrate;

a second device having a gate disposed on a gate dielectric layer having the first thickness and the first effective gate dielectric value, the gate dielectric layer fabricated on a semiconductor substrate, a buried channel implanted below the gate dielectric layer, the buried channel being doped with a predetermined dopant and a peak concentration of the dopant positioned at a selected level in the substrate below the gate dielectric layer to cause the substrate portions above the selected level to act as a supplemental gate dielectric layer to increase the effective gate dielectric thickness of the second device, wherein the level is selected so that the effective gate dielectric thickness of the second device is a predetermined value greater than the first effective gate dielectric value.

24. (previously added) The integrated circuit as recited in claim 23 wherein the insulating gate dielectric layer and the substrate forms an interface and the peak concentration of implanted dopants in the buried channel is located between 400 and 1000 Angstroms below the interface.

25. (previously added) The integrated circuit as recited in claim 23 wherein the device is a MOS capacitor.

26. (previously added) The integrated circuit as recited in claim 23 wherein the substrate is a p-type substrate and the buried channel is an n-type buried channel.